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PATENT

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On 9/15/03

TOWNSEND and TOWNSEND and CREW LLP

By: *Lisa Haines*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Maria C. Y. Quinones, et al.

Application No.: 09/487,969

Filed: January 18, 2000

For: IMPROVED METHOD OF  
MAKING A CHIP DEVICE

Examiner: Alonzo Chambliss

Art Unit: 2814

**DECLARATION UNDER  
37 C.F.R. § 1.131**

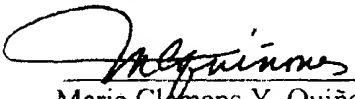
Sir:

We, Maria Clemens Y. Quinones, Gilmore S. Baje, Maria Cristina B. Estacio, Marvin R. Gestole, Oliver M. Ledon, and Santos Mepieza, each declare as follows:

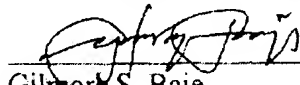
1. I am a co-inventor of at least one claim in the referenced patent application.
2. I have reviewed the Office Action mailed on December 31, 2002, and the obviousness rejections of claims 7-33 based on U.S. Patent No. 6,307,755 to Williams et al.
3. The inventions of at least pending independent claims 7, 15, and 23 were conceived of before May 27, 1999, the filing date of Williams et al. Evidence of conception is shown by the attached documents in Exhibit A. Some of the pages in Exhibit A include initials and dates of January 5 and 6, 1999.

4. Reduction to practice of embodiments of the inventions before May 27, 1999, is evidenced by the documents in Exhibits B and C, which include e-mail communications between one or more co-inventors and others. A die package that was produced according to an embodiment of the invention was referred to internally at Fairchild Semiconductor as "SO-8" wireless. As evidence of reduction to practice, one e-mail communication in Exhibit B states "Wireless samples (SO-8) were sent from Steve Sapp with objective of identifying source of Rdson lower than expected." One e-mail in Exhibit C states "Add top & bottom alignment press-fit studs & holes ... Status: Changes incorporated in Rev. P bottom frame and Rev. N topframe design." The documents in Exhibits B and C were originally created before May 27, 1999 and show that an embodiment of the invention was reduced to practice before May 27, 1999.
5. Exhibit D contains correspondence regarding the preparation of a patent application for embodiments of the invention. The correspondence includes: a letter dated June 4, 1999 from Fairchild Semiconductor to Townsend, Townsend & Crew (TTC) requesting the preparation of a patent application; a letter dated June 7, 1999 from TTC acknowledging receipt of the June 4, 1999 letter; a file note dated September 20, 1999 with some invention details; a letter dated November 19, 1999 from TTC to Ms. Quinones with a draft patent application; and an e-mail dated December 5, 1999 with comments on the prior draft patent application.
6. As shown by Exhibits A-C, I believe that an embodiment of the invention was conceived of and reduced to practice before May 27, 1999. As shown by Exhibits A-D, embodiments of the invention were also conceived of before May 27, 1999 and were diligently pursued until the filing of the present application.


7. The acts relied on in this Declaration (and described in the Exhibits) took place in a WTO country.
8. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. §1001) and may jeopardize the validity of the application or any patent issuing thereon.

  
\_\_\_\_\_  
Maria Clemens Y. Quiñones

\_\_\_\_\_  
Date

  
\_\_\_\_\_  
Gilmore S. Baje


\_\_\_\_\_  
Date

  
\_\_\_\_\_  
Maria Cristina B. Estacio

\_\_\_\_\_  
Date

  
\_\_\_\_\_  
Marvin R. Gestole

\_\_\_\_\_  
Date

  
\_\_\_\_\_  
Oliver M. Ledon

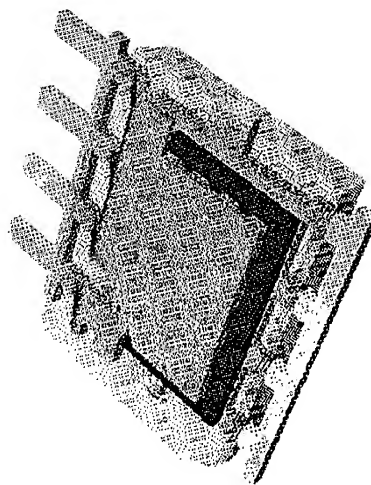
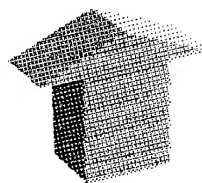
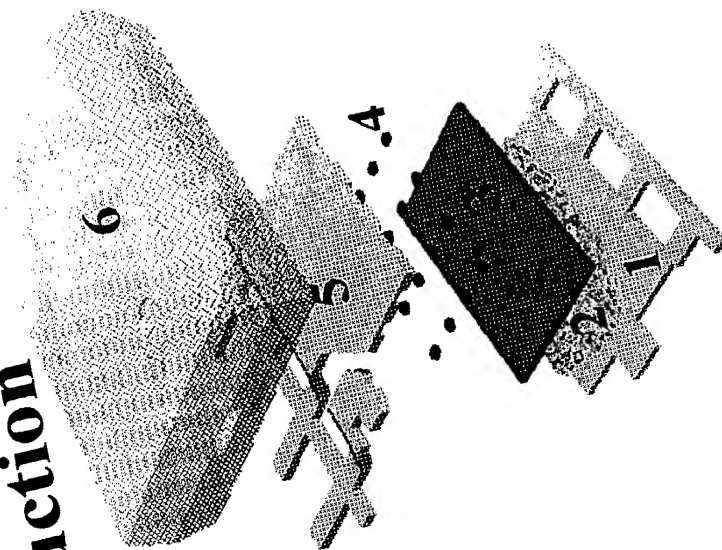
\_\_\_\_\_  
Date

  
\_\_\_\_\_  
Santos Mepieza

\_\_\_\_\_  
Date

**FAIRCHILD**  
SEMICONDUCTOR

# SOIC-8 DMOS High-Performance Construction Package Construction



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# High-Performance SOIC-8 DMOS Package Construction

## SUMMARY

### Part 6 : SOIC-8 Molded Outline

- Length = 0.193" typ
- Width = 0.154" typ
- Thickness = 0.057" typ

### Part 5 : Gate & Source Terminal Contacts

### Part 4 : Solder Bumps

- Bump Alloy: Pb/Sn or Pb/Sn/Ag or Sn/Sb
- Bump diameter ~ 0.008"
- Bump Height ~ 0.006"
- UBM: TiW/Cu/Au or equivalent

### Part 3 : FSC DMOS Trench Die with Source & Gate Array

### Part 2 : Die Attach Material

- Ag-filled Adhesives (Epoxy, polyimide)
- Soft Solder

### Part 1 : Die Attach Pad

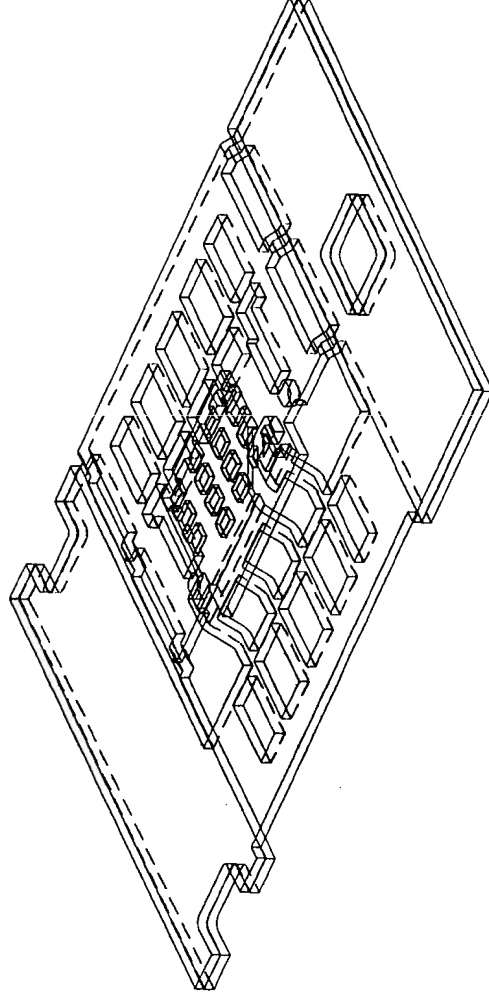
- Material: Cu alloy
- DAP plating options: None, Ag, Ni
- DAP support:
  - X-axis: tie bars
  - Y-axis: Drain terminals

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*Ag-filled I Jan '99*  
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*Ag-filled I Jan '99*  
*Ag-filled I Jan '99*  
*Ag-filled I Jan '99*



# High-Performance SOIC-8 DMOS Leadframe Design



**FSC Confidential**




## BOTTOM LEADFRAME

| Leadframe Part       | Function  |
|----------------------|---|
| DAP                  | Die Attach Pad; Drain connection;                                 |
| Tie Bar              | DAP support; Package support @ lead stage forming                 |
| Dambar               | Mold flash barrier  |
| Drain Leads          | Drain terminals   |
| Rail Upset           | Levels drain leads with gate & source leads                       |
| Index/Alignment Hole | Transport handling feature; Alignment for top & bottom leadframes |
| Rail                 | Backbone or main mechanical support of leadframe                  |

*John* 5 Jan '99  
*Regina* 5 Jan '99  
*John* 5 Jan '99  
*John* 5 Jan '99  
*John* 5 Jan '99  
*John* 5 Jan '99

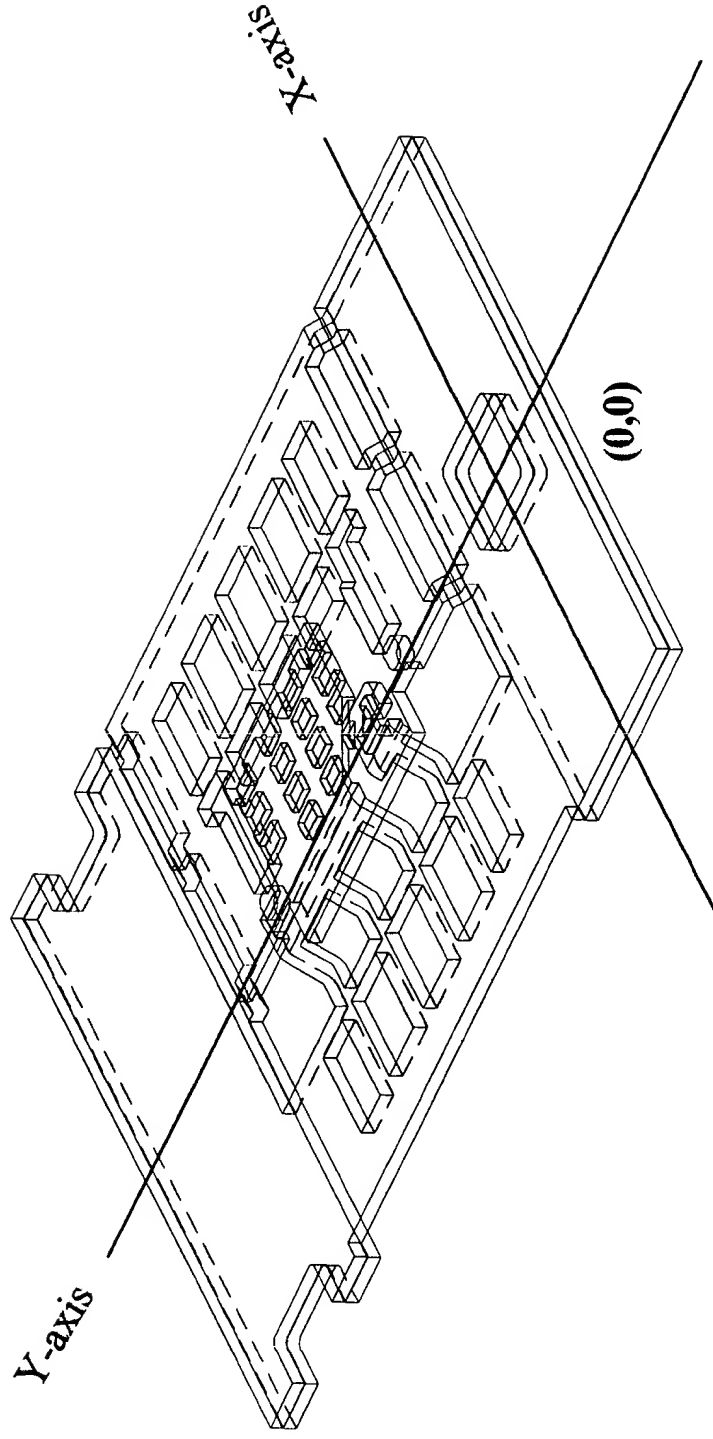
## TOP LEADFRAME

| Leadframe Part       | Function  |
|----------------------|---|
| Source Pad           | Connect 3 terminals to source metallizations of die                   |
| Gate Pad             | Connect 1 terminal to gate metallization of die                       |
| Contact Protrusions  | Provide good contact between solder bumps of die and source/gate pads |
| Dambar               | Mold flash barrier; Leads coplanarity support                         |
| Lead Upset           | Provides space for solder bumped die                                  |
| Index/Alignment Hole | Transport handling feature; Alignment for top & bottom leadframes     |
| Rail                 | Backbone or main mechanical support of leadframe                      |

 5 JAN '99  
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 (Rev. 1.1) 5 Jan '99



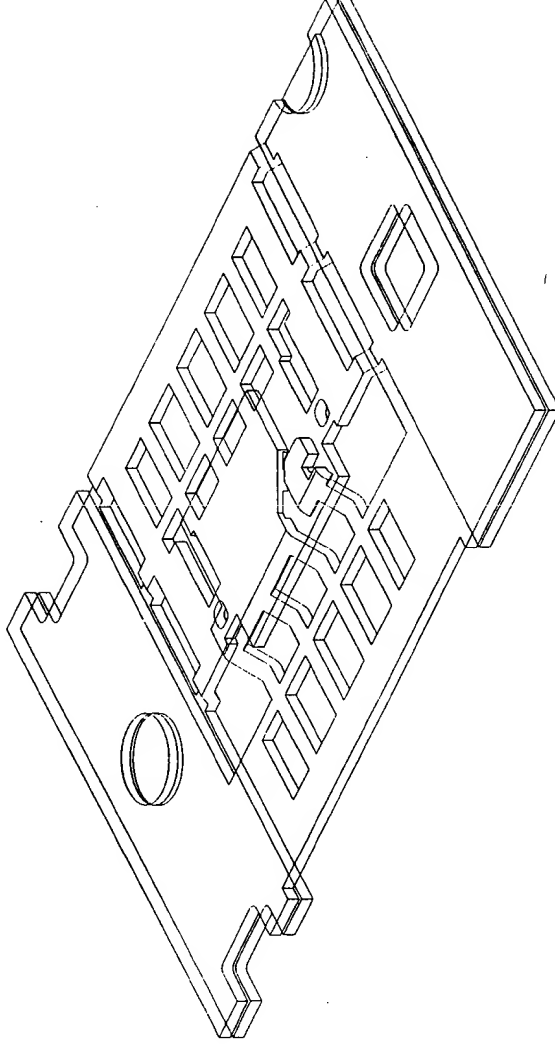
## Top & Bottom Leadframe Assembly



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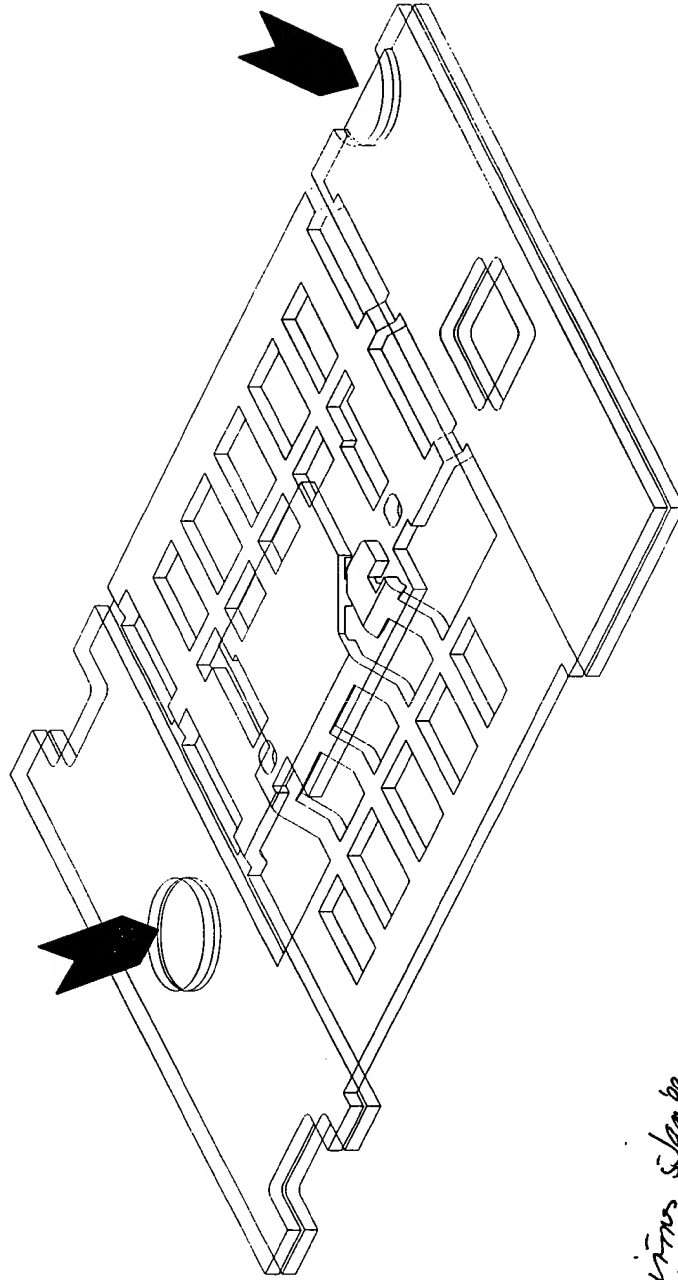


# High-Performance SOIC-8 DMOS Leadframe Easy-Align Feature



## TOP & BOTTOM LEADFRAME ASSEMBLY

Bottom Frame Aligners are press-fitted unto top frame alignment holes keeping both leadframes steadily stacked. Press fitting can be integrated right after top frame attach



*McQuinn, Sean 4/9*  
*5/2/99*  
*5/2/99*  
*5/2/99*  
*5/2/99*

# HIGH PERFORMANCE SOIC-8 DMOS PROCESS FLOW FRONT END ASSEMBLY OPTIONS (Summary)

|        | OPTION<br>1           | OPTION<br>2               | OPTION<br>3                                   | OPTION<br>4                                   | OPTION<br>5                 | OPTION<br>6                                   | OPTION<br>7            | OPTION<br>8               |
|--------|-----------------------|---------------------------|---|---|-----------------------------|---|------------------------|---------------------------|
| Step 1 | Epoxy Die<br>Attach   | Soft Solder Die<br>Attach | Top Frame<br>Fluxing                          | Top Frame<br>Fluxing                          | Epoxy Die<br>Attach         | Top Frame<br>Fluxing                          | Epoxy Die<br>Attach    | Soft Solder Die<br>Attach |
| Step 2 | Epoxy Cure            | Top Frame<br>Fluxing      | Flip Chip<br>Attach                           | Flip Chip<br>Attach                           | Epoxy Cure                  | Flip Chip<br>Attach                           | Epoxy Cure             | Solder Bump<br>Fluxing    |
| Step 3 | Top Frame<br>Fluxing  | Top Frame<br>Attach       | Solder Bump<br>Reflow                         | Solder Bump<br>Reflow                         | Top Frame<br>Screen Fluxing | Bottom Frame<br>Solder Paste<br>Dispense      | Solder Bump<br>Fluxing | Top Frame<br>Attach       |
| Step 4 | Top Frame<br>Attach   | Solder Bump<br>Reflow     | Bottom Frame<br>Epoxy<br>Dispense             | Bottom Frame<br>Solder Paste<br>Dispense      | Bottom Frame<br>Loading     | Top & Bottom<br>Frame<br>Sandwich<br>Assembly | Top Frame<br>Attach    | Rail Spot<br>Welding      |
| Step 5 | Solder Bump<br>Reflow |                           | Top & Bottom<br>Frame<br>Sandwich<br>Assembly | Top & Bottom<br>Frame<br>Sandwich<br>Assembly | Top Frame<br>Loading        | Rail Spot<br>Welding                          | Rail Spot<br>Welding   | Solder Bump<br>Reflow     |
| Step 6 |                       |                           | Epoxy Cure                                    |   | Rail Spot<br>Welding        |   | Solder Reflow          |                           |
| Step 7 |                       |                           |   |   | Solder Bump<br>Reflow       |   |                        |                           |

*James C Jan '99*  
*Longth 5 Jan '99*  
*Chen 5 Jan '99*  
*Macquinn 5 Jan '99*  
*Wong 5 Jan '99*  
*Antoni 1 Jan '99*



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

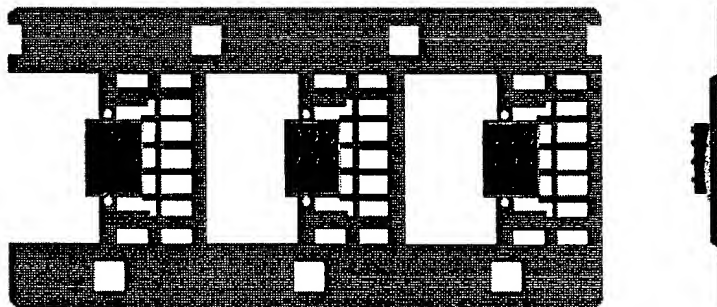
FRONT END ASSEMBLY, OPTION 1

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1



## EPOXY DIE ATTACH

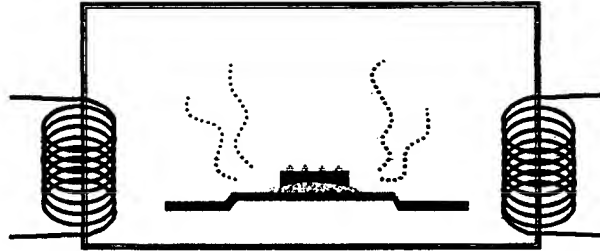


Precise die placement required @ +/- 2 mils accuracy.

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2

## EPOXY CURE

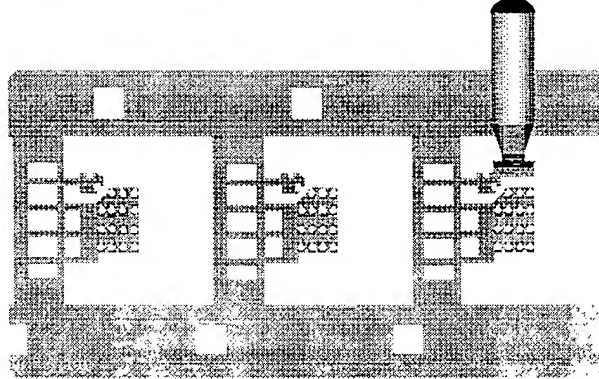


Options: conventional box oven curing, heater block snap curing, or equivalent

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3

## TOP FRAME FLUXING

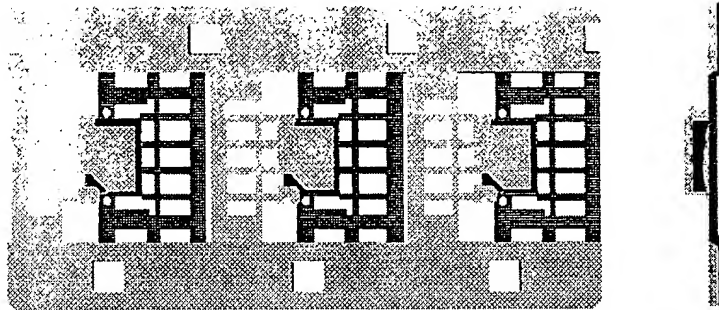


Top frame fluxing done with gate & source contact pads facing up.

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4

## TOP FRAME ATTACH

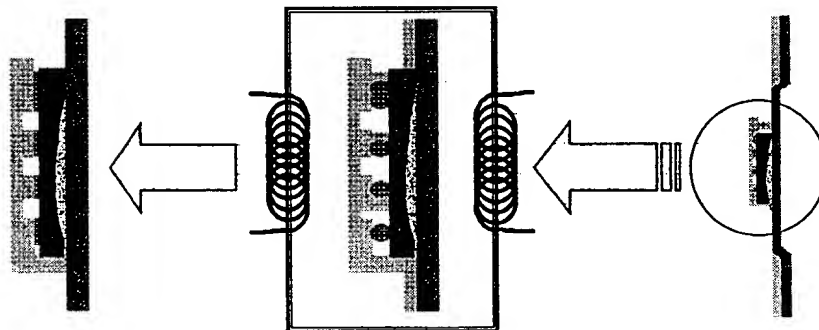


**Top frame is flipped and mounted to bottom frame assembly.**

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5

## SOLDER REFLOW



**Top & bottom frame sandwich assembly are heated to reflow the solder bumps and permanently attach die to the topframe.**

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6



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

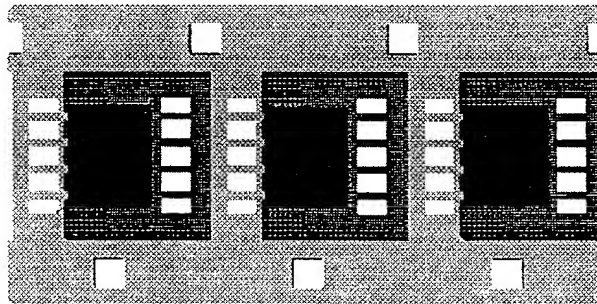
END OF LINE ASSEMBLY, OPTION 1

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1



## MOLDING



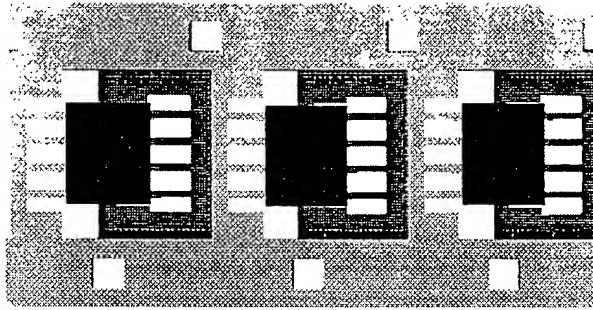
SOIC-8 wireless assembly is molded with die facing up.

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2



## DEBAR & DEJUNK

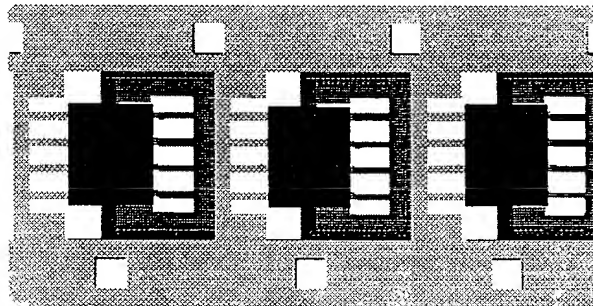


**Dambar & mold flashes are mechanically removed.**

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3

## MEDIA DEFLASH

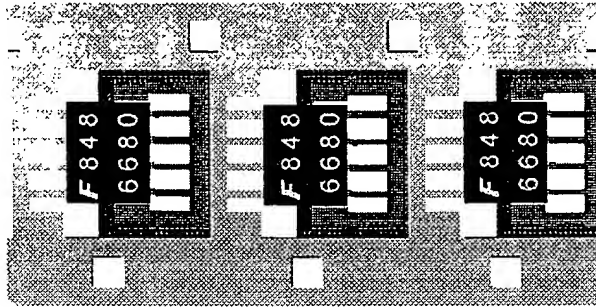


**Remaining resin bleeds on leads are removed using  
pressurized media deflash grits.**

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4

## LASER MARKING



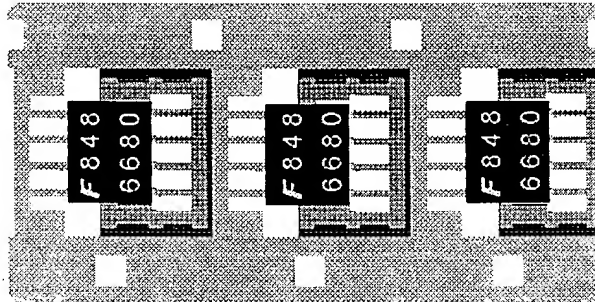
**Laser marking is done stripwise.**

NOTE: Sample marking only; context with no definite meaning.

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5

## POSTPLATE



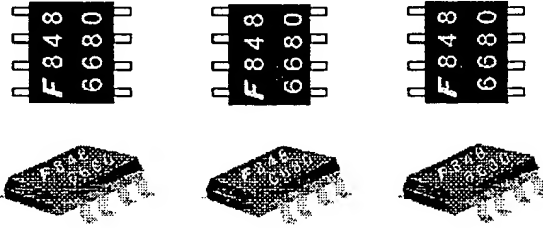
**Rack plating**

NOTE: Sample marking only; context with no definite meaning.

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6

## TRIM & FORM



### 3-stage forming

NOTE: Sample marking only; context with no definite meaning.

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7



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

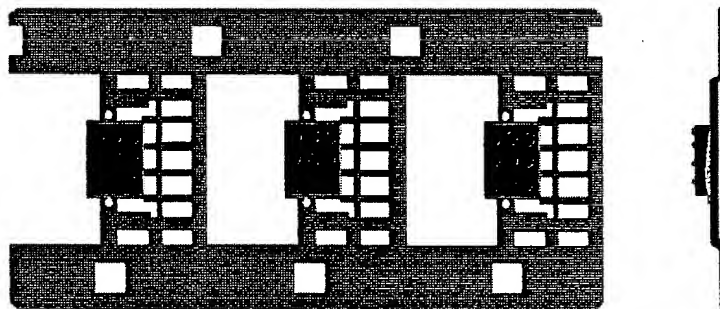
### FRONT END ASSEMBLY, OPTION 2

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1



## SOFT SOLDER DIE ATTACH



Precise die placement required @ +/- 2 mils accuracy.

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2

## TOP FRAME FLUXING

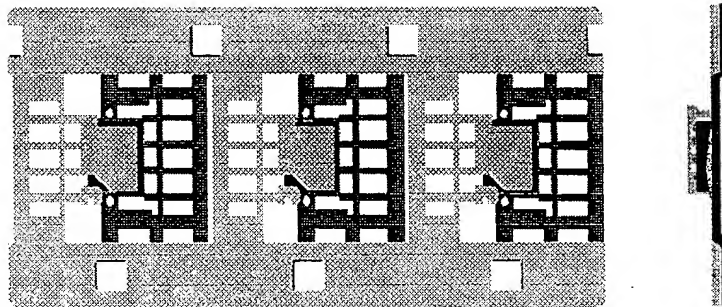


**Top frame fluxing done with gate & source contact pads facing up.**

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3

## TOP FRAME ATTACH

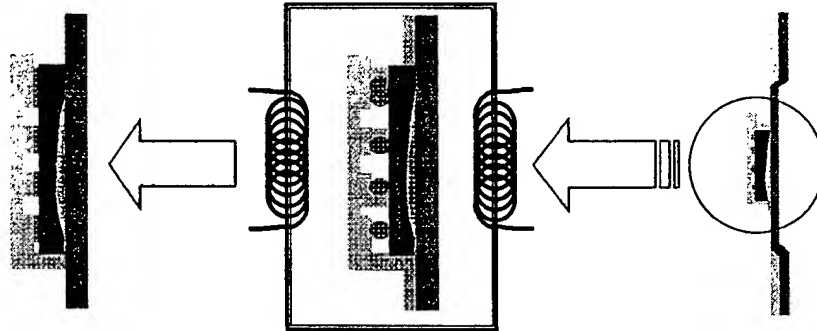


**Top frame is flipped and mounted to bottom frame assembly.**

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4

## SOLDER BUMP REFLOW



**Top & bottom frame sandwich assembly are heated to reflow the solder bumps and permanently attach die to the topframe.**

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5



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

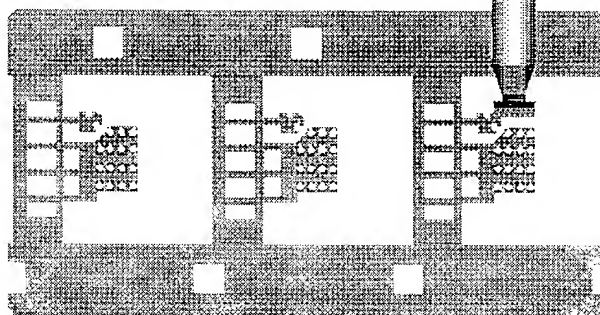
### FRONT END ASSEMBLY, OPTION 3

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1



## TOP FRAME FLUXING

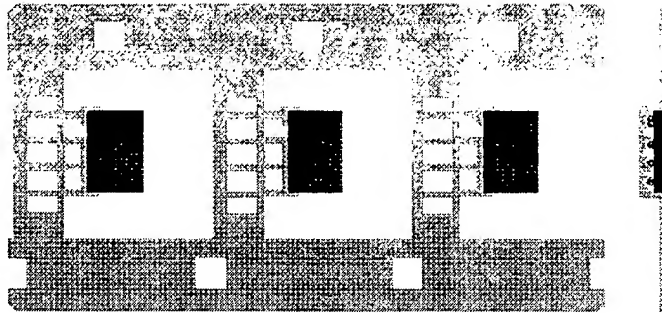


Top frame fluxing done with gate & source contact pads facing up.

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2

## FLIP CHIP ATTACH

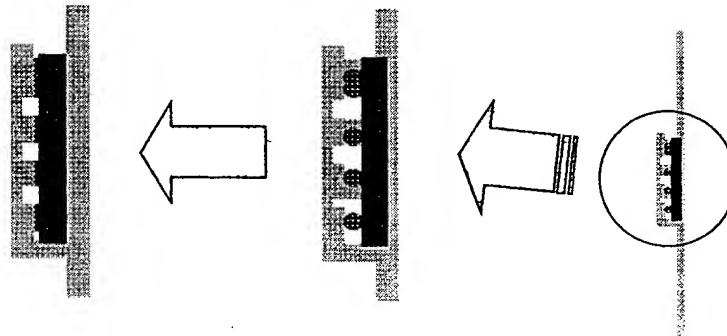


Die is flipped from its pick-up position & attached solder bumps facing down to the top frame. Die placement precision requirement is  $\pm 2$  mils.

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3

## SOLDER BUM PREFLOW



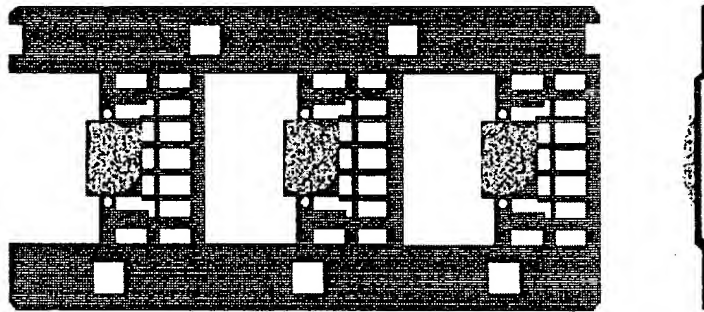
Flipped die & topframe are heated to reflow the solder bumps and permanently attach die to the topframe.

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4



## BOTTOM FRAME EPOXY DISPENSE

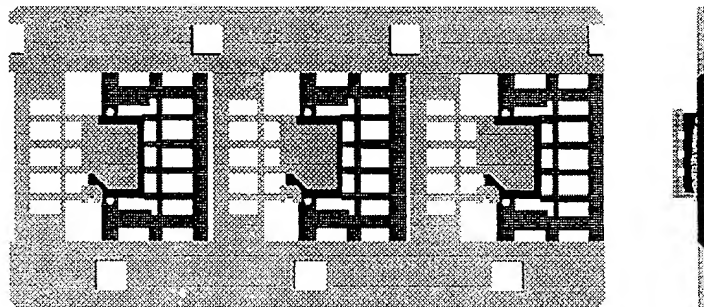


Conductive epoxy is dispensed on die attach pad.

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5

## TOP & BOTTOM FRAME SANDWICH ASSEMBLY

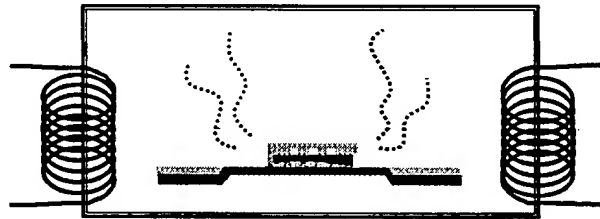


Flip chip attached top frame is flipped over bottom frame to complete SOIC-8 wireless assembly. Precise alignment is required.

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6

## EPOXY CURE



Options: conventional box oven curing, heater block snap curing, or equivalent

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7



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

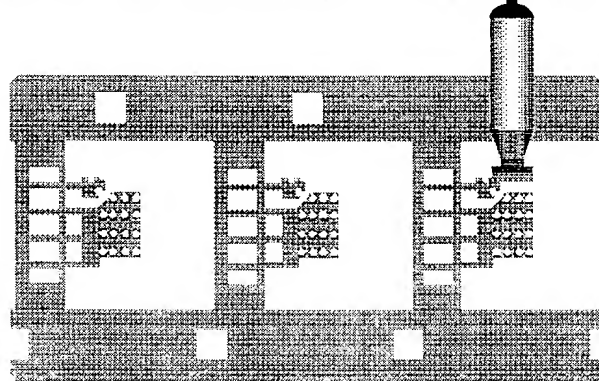
### FRONT END ASSEMBLY, OPTION 4

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1



## TOP FRAME FLUXING

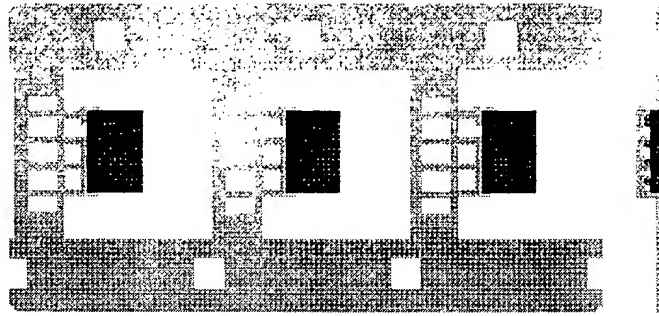


Top frame fluxing done with gate & source contact pads facing up.

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2

## FLIP CHIP ATTACH

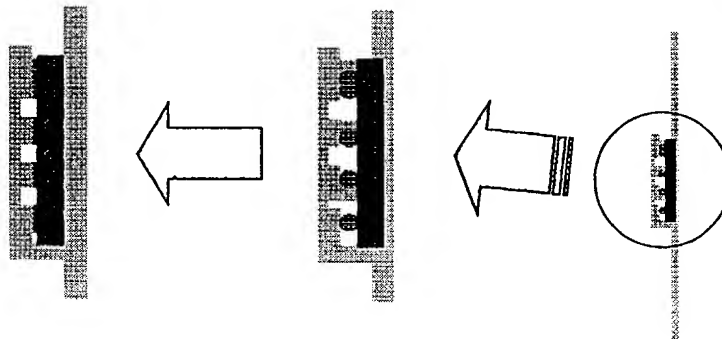


**Die is flipped from its pick-up position & attached solder bumps facing down to the top frame. Die placement precision requirement is +/- 2 mils.**

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3

## SOLDER BUMP REFLOW

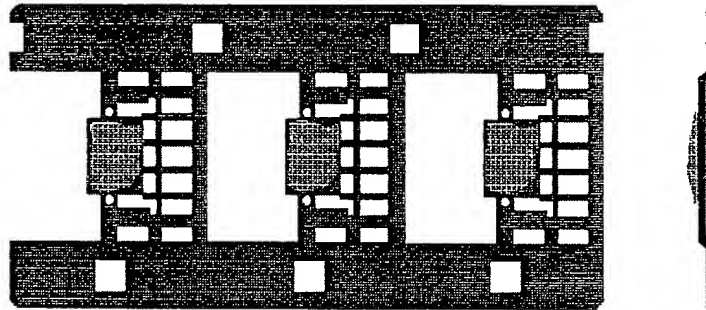


**Flipped die & topframe are heated to reflow the solder bumps and permanently attach die to the topframe.**

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4

## BOTTOM FRAME SOLDER PASTE DISPENSE

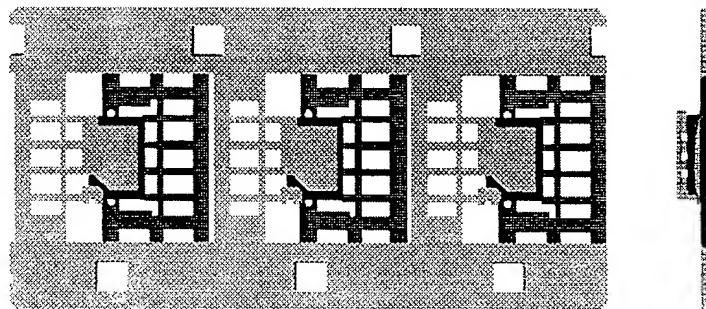


Low melting solder paste (relative to die solder bump) is dispensed on die attach pad.

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## TOP & BOTTOM FRAME SANDWICH ASSEMBLY



Flip chip attached top frame is flipped over bottom frame to complete SOIC-8 wireless assembly. Precise alignment is required. Whole assembly is done on a heated block.

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6



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

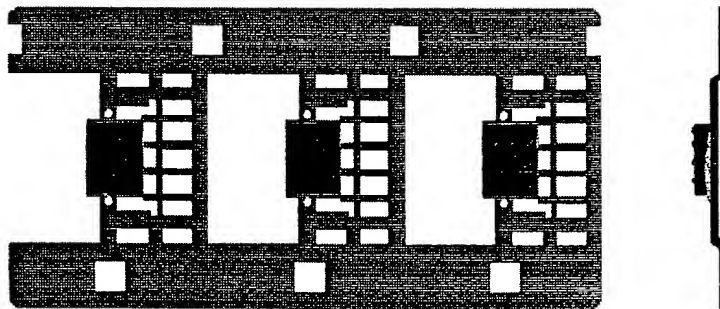
FRONT END ASSEMBLY, OPTION 5

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1



## EPOXY DIE ATTACH

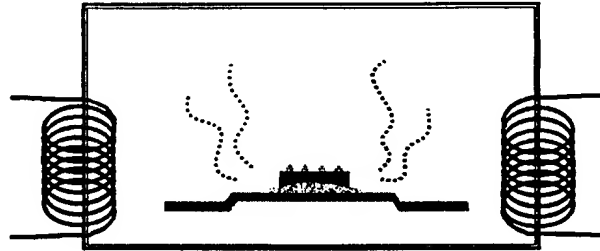


Precise die placement required @ +/- 2 mils accuracy.

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2

## EPOXY CURE

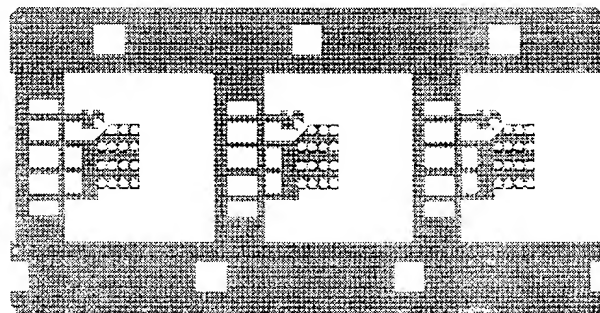


Options: conventional box oven curing, heater block snap curing, or equivalent

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3

## TOP FRAME SCREEN FLUXING

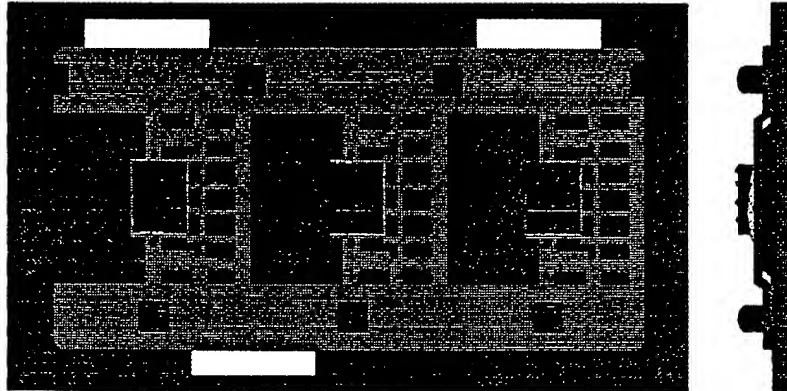


Top frame fluxing done with gate & source contact pads facing up.

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4

## BOTTOM FRAME LOADING

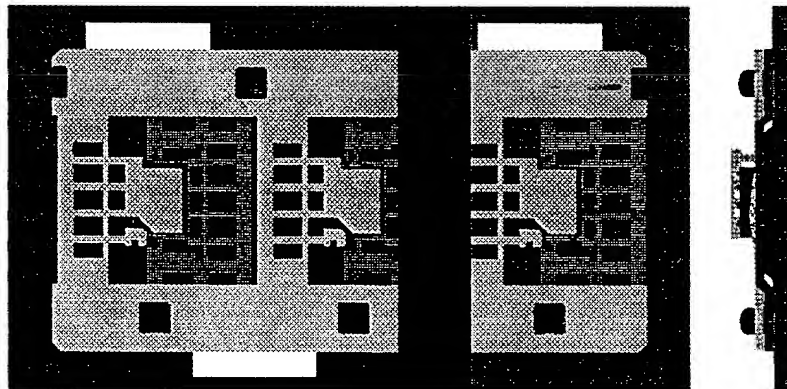


**Bottom frame is loaded on work loading frame.**

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5

## TOP FRAME LOADING



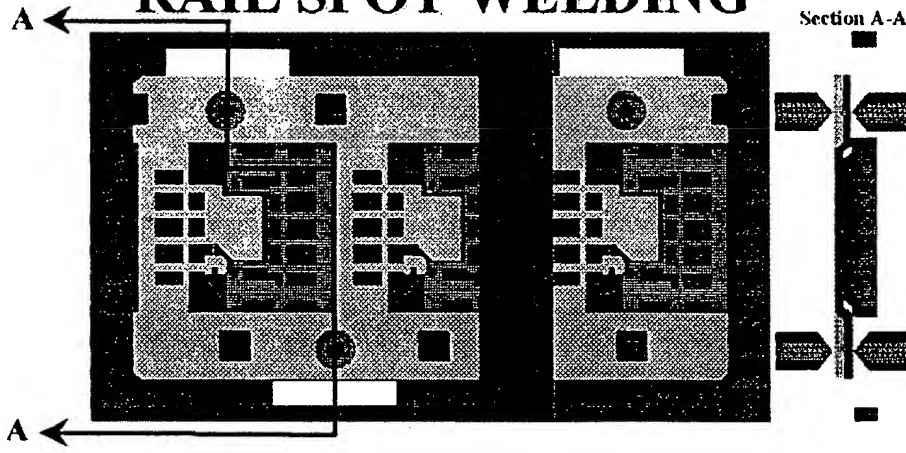
**Fluxed top frame is flipped & loaded on top of bottom frame;  
after which, work loading frame is locked.**

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6



## RAIL SPOT WELDING

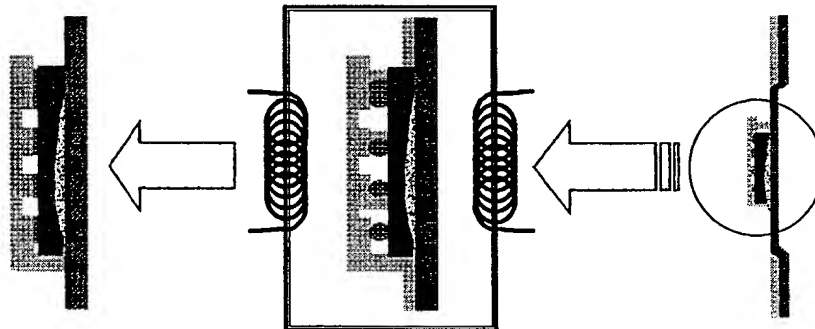


Top & bottom leadframe rails are spot welded together.

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7

## SOLDER REFLOW



Top & bottom leadframe sandwich assembly are heated to reflow the solder bumps and permanently attach die to the topframe.

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8



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

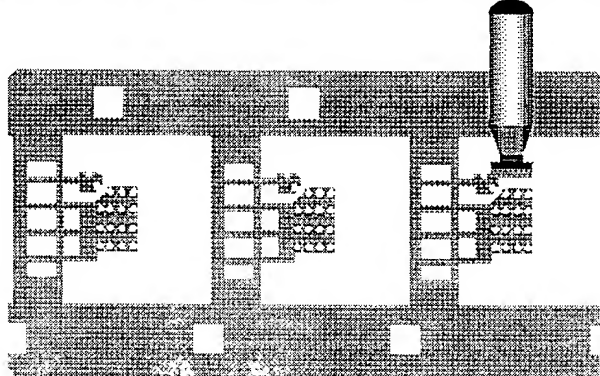
### FRONT END ASSEMBLY, OPTION 6

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1



## TOP FRAME FLUXING

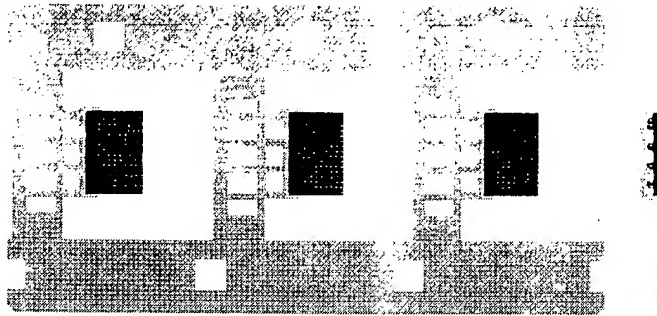


Top frame fluxing done with gate & source contact pads facing up.

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2

## FLIP CHIP ATTACH

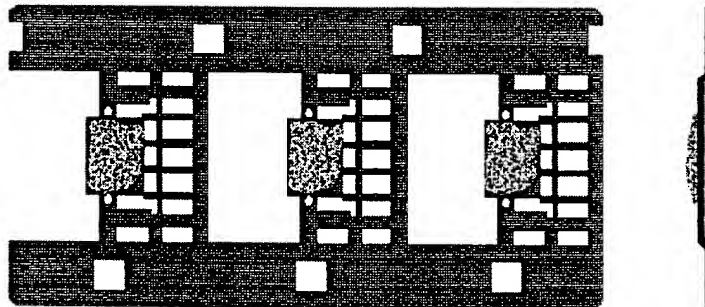


Die is flipped from from its pick-up position & attached solder bumps facing down to the top frame. Die placement precision requirement is  $\pm 2$  mils.

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3

## BOTTOM FRAME SOLDER PASTE DISPENSE

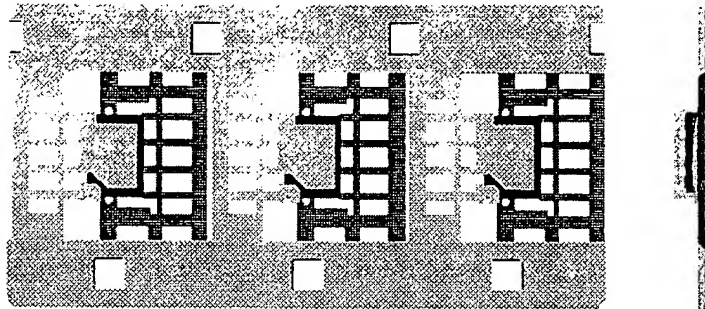


Low melting solder paste is dispensed on die attach pad.

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4

## TOP & BOTTOM FRAME SANDWICH ASSEMBLY

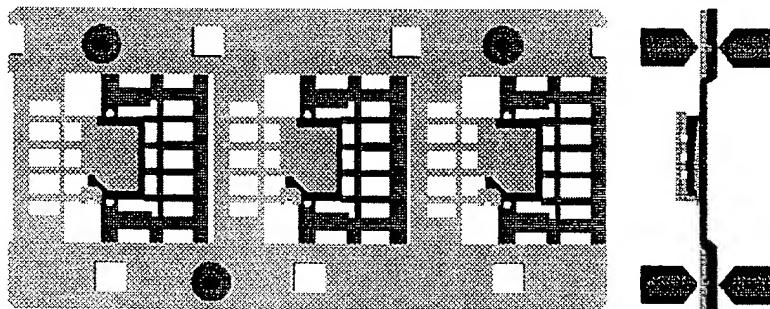


Flip chip attached top frame is flipped over bottom frame to complete SOIC-8 wireless assembly. Precise alignment is required. Whole assembly is done on a heated block.

FSC Confidential

5

## RAIL SPOT WELDING



Top & bottom leadframe rails are spot welded together.

FSC Confidential

6



## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

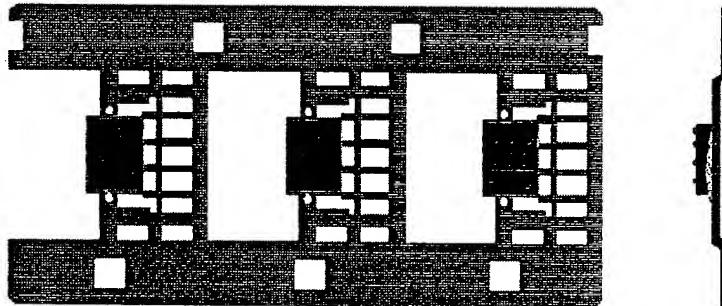
FRONT END ASSEMBLY, OPTION 7

FSC Confidential

1



## EPOXY DIE ATTACH

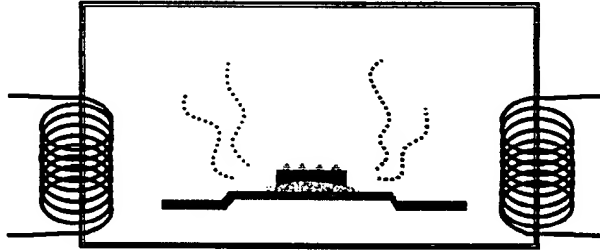


Precise die placement required @ +/- 2 mils accuracy.

FSC Confidential

2

## EPOXY CURE

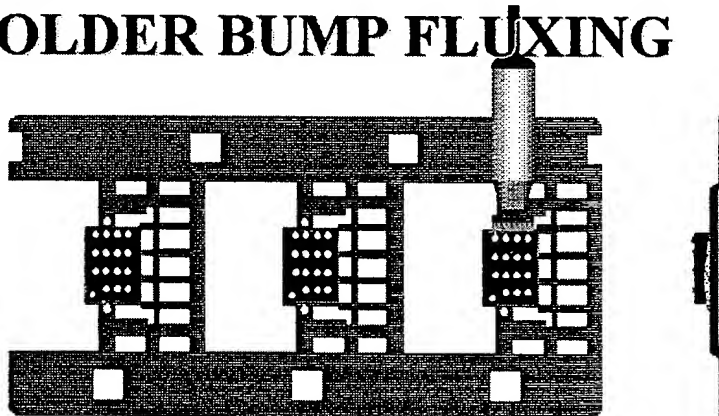


Options: conventional box oven curing, heater block snap curing, or equivalent

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3

## SOLDER BUMP FLUXING

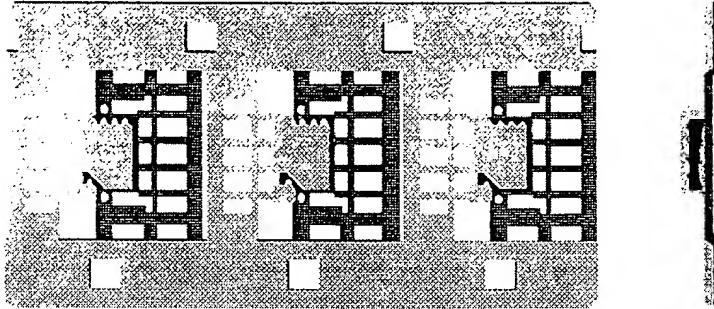


Solder bumps are dispensed with small amount of flux.

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4

## TOP FRAME ATTACH

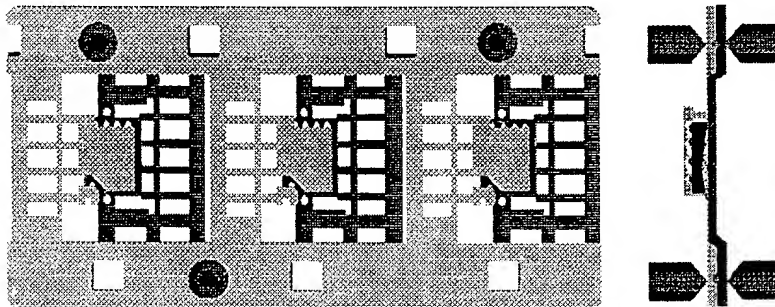


Top frame is mounted to bottom frame assembly.

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5

## RAIL SPOT WELDING

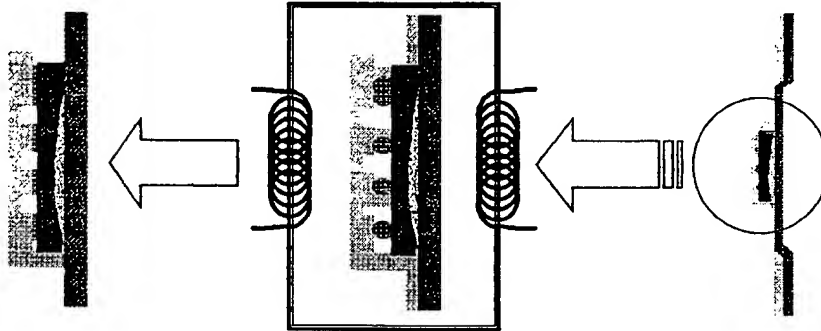


Top & bottom leadframe rails are spot welded together.

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6

## SOLDER REFLOW



**Top & bottom frame sandwich assembly are heated to reflow the solder bumps and permanently attach die to the topframe.**

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7





## HI-PERFORMANCE SOIC-8 DMOS

# PROCESS FLOW

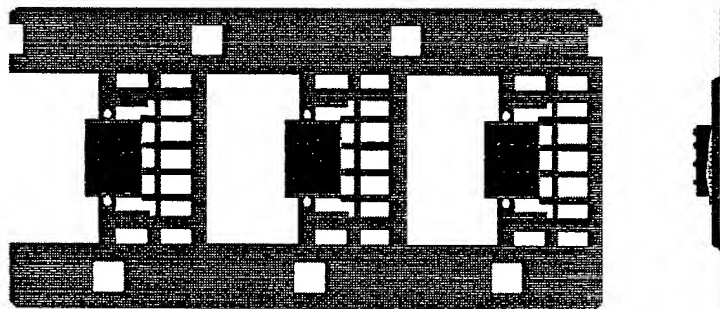
FRONT END ASSEMBLY, OPTION 8

FSC Confidential

1



## SOFT SOLDER DIE ATTACH

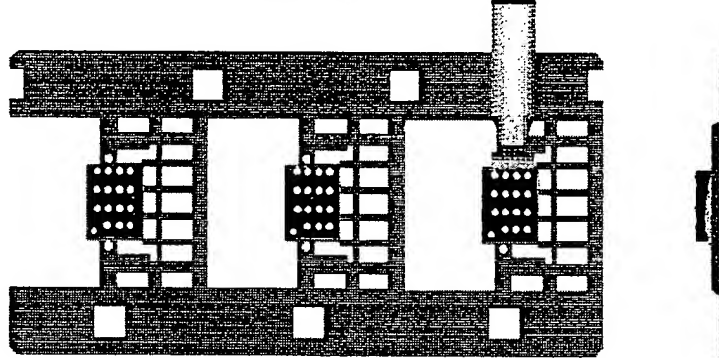


Precise die placement required @ +/- 2 mils accuracy.

FSC Confidential

2

## SOLDER BUMP FLUXING

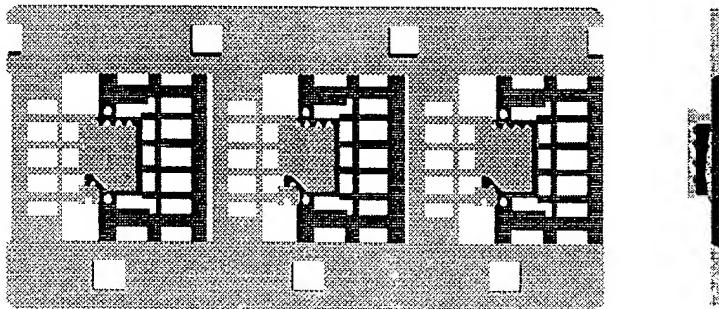


Solder bumps are dispensed with small amount of flux.

FSC Confidential

3

## TOP FRAME ATTACH

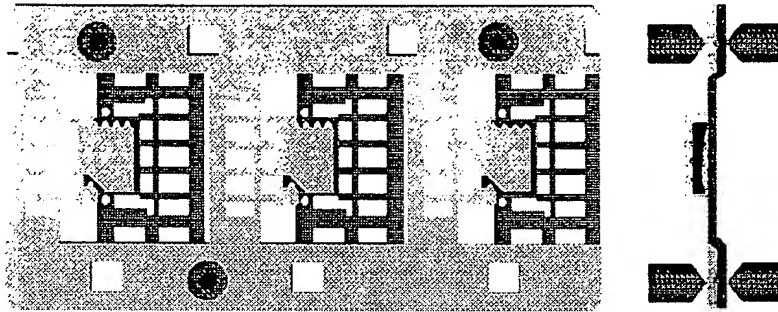


Top frame is mounted to bottom frame assembly.

FSC Confidential

4

## RAIL SPOT WELDING

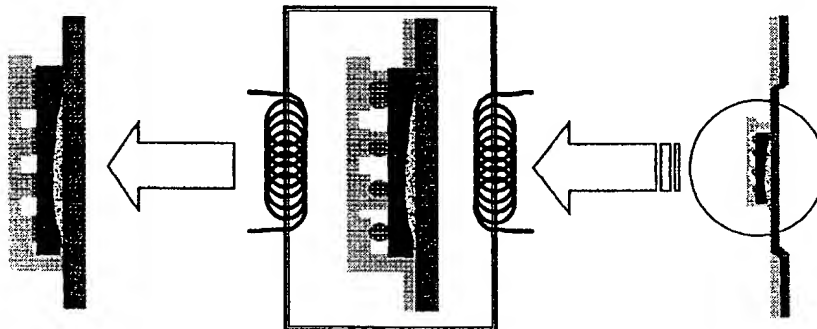


Top & bottom leadframe rails are spot welded together.

FSC Confidential

5

## SOLDER REFLOW



Top & bottom frame sandwich assembly are heated to reflow the solder bumps and permanently attach die to the topframe.

FSC Confidential

6

## Response

Subject: >SO-8 Wireless Internal Pkg Characterizations in Salt Lake  
 Response to: EVALUATIONS & LEARNINGS  
 Category: Wireless SO-8 Pkg Dev't (Single Strand Approach)

**Report 2/5 - Wireless SO-8**

----- Forwarded by Steve Pritchett/SaltLake/Fairchild on 04/21/99 06:32 PM -----



Steve Pritchett  
 04/21/99 03:29 PM

To: Rajeev Joshi/SantaClara/Fairchild@Fairchild, Ma Cristina B Estacio/Cebu/Fairchild@Fairchild, Consuelo N Tangpuz/Cebu/Fairchild@Fairchild, Honorio T Granada Jr/Cebu/Fairchild@Fairchild, Lester O Uy/Cebu/Fairchild@Fairchild  
 cc: Steven Sapp/SantaClara/Fairchild@Fairchild, Bruce Marchant/SaltLake/Fairchild@Fairchild, John R Diroll/SaltLake/Fairchild@Fairchild, R Evan Bendall/SaltLake/Fairchild@Fairchild, Henry W Hurst/SaltLake/Fairchild@Fairchild, Annette Pieper/SaltLake/Fairchild@Fairchild, Gordon Madson/SaltLake/Fairchild@Fairchild  
 Subject: Report 2/5 - Wireless SO-8

I have broken this up into 4 emails/reports due to many photos.

1. Flipchip samples, some with gate to source shorts, some with black "corrosion" stain. (sent 4-19)
2. **Wireless samples from Steve Sapp, SO-8 good/bad?, identify cause of high Rdson.**
3. SO-8 wireless samples prior to molding, sent per SL request to help understand leadframe layout.
4. Bare die samples with bumps, sent per SL request.
5. Samples of SOT-223 wireless parts sent to SV, construction analysis. (still in que)

Wireless samples (SO-8) were sent from Steve Sapp with objective of identifying source of Rdson lower than expected. Previous email sent 3-24-99 showing poor UBM to Al pad contact area, leadframe not contacting all bumps and D/A voids (w/ epoxy attach, not standard).

**SUMMARY - Same as above just more photos of leadframe alignment and spacing affects.**  
**Wicking of solder into molding compound channel could be problem for controlling bump size.**  
**Note: JPG files for these photos are available upon request.**

As received, some of the parts were labeled good, some bad. We assume this related to Rdson measurement.

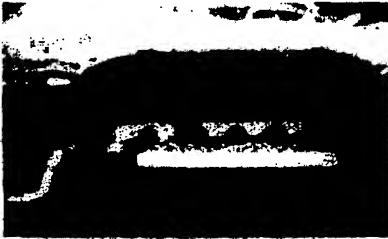
The following photos are observations. Cebu will need to access if these are problems, not representative of current process, etc.



This is part # 206, no contact , bump to leadframe at left side. (wire-206a.jpg)



This is part # 206, more bumps contacting than above photo on different bump row. Indicates angled front to back as well as angle side to side shown above. (wire-206b.jpg)



This is part # 245 showing gate pad. Gate leadframe appears to be at different angle than source leadframe. (wire-245a.jpg)



This is part # 245, good horizontal alignment, but assume "squished" bumps? What is desired/acceptable profile? (wire-245b.jpg)

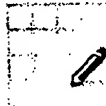


This is part #260. It appears the surface condition of the bump contact leadframe will allow the solder to wick into molding compound channel. Could make bump size and volume difficult to control. The "squished" bumps may allow the bump metal to extend over non-common die metal. For example, a squished gate bump may result in overlap over source metal. Steve Sapp had voiced the opinion that this overlap was unacceptable due to concern with passivation integrity (although it looks like new Fujitsu layout will overlap the UBM over source Al). (wire-260.jpg)

Thanks to Wayne Hurst and Ann te Pieper for sample preparation , photos and input for this write-up.  
They are a little backed up for FA work at present.  
Thanks, Steve

**Report 3/5 - Wireless SO-8**

----- Forwarded by Steve Pritchett/SaltLake/Fairchild on 04/21/99 06:32 PM -----



Steve Pritchett  
04/21/99 03:31 PM

To: Rajeev Joshi/SantaClara/Fairchild@Fairchild, Ma Cristina B Estacio/Cebu/Fairchild@Fairchild, Consuelo N Tangpuz/Cebu/Fairchild@Fairchild, Honorio T Granada Jr/Cebu/Fairchild@Fairchild, Lester O Uy/Cebu/Fairchild@Fairchild  
cc: Steven Sapp/SantaClara/Fairchild@Fairchild, Bruce Marchant/SaltLake/Fairchild@Fairchild, John R Diroll/SaltLake/Fairchild@Fairchild, R Evan Bendall/SaltLake/Fairchild@Fairchild, Henry W Hurst/SaltLake/Fairchild@Fairchild, Annette Pieper/SaltLake/Fairchild@Fairchild, Gordon Madson/SaltLake/Fairchild@Fairchild  
Subject: Report 3/5 - SO-8 Leadframe

I have broken this up into 4 emails/reports due to many photos.

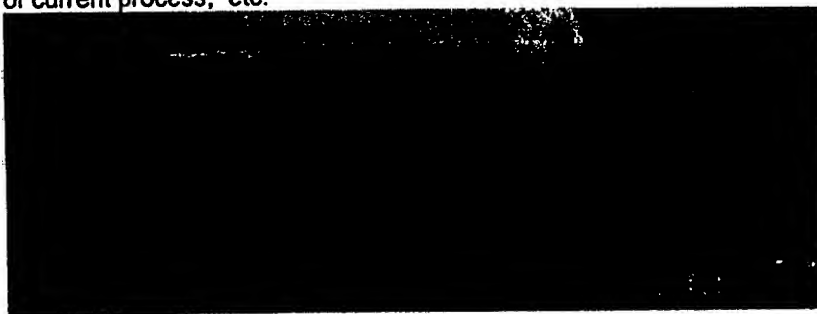
1. Flipchip samples , some with gate to source shorts, some with black "corrosion" stain. (sent 4-19)
2. Wireless samples from Steve Sapp, SO-8 good/bad ?, identify cause of high Rdson. (sent 4-20)
3. **SO-8 wireless samples prior to molding, sent per SL request to help understand leadframe layout.**
4. Bare die samples with bumps, sent per SL request.
5. Samples of SOT-223 wireless parts sent to SV, construction analysis. (still in que)

SO-8 wireless leadframe samples were sent from Cebu with objective of allowing SL to view assembly components.

**SUMMARY - Good photo of Al metal not covered by UBM or passivation. D/A die position appears to be highly variable and source of bump to leadframe alignment variation.**

As received, the parts had been through bump reflow, but not molded.

The following photos are observations. Cebu will need to access if these are problems, not representative of current process, etc.



This shows bump and passivation opening at edge of bump. Al metal is not protected! (s08lf3.jpg & s08lf1.jpg)



Interesting photo of crack beginning across bump. This part was manually cut from leadframe strip prior to SEM. Crack may have been caused by singulation? (so8lf2.jpg)



(so8lf12t.jpg & so8lf12e.jpg)



(so8lf14t.jpg & so8lf14e.jpg)




These three sets of photos show the variation in horizontal die position along with impact to bump alignment. Gate bump appears to be fully "squished" in photos. Stress relief for squished bumps is probably minimal. (so8lf16t.jpg & so8lf16e.jpg)

Thanks to Wayne Hurst and Annette Pieper for sample preparation , photos and input for this write-up. They are a little backed up for FA work at present.

Thanks, Steve

**Report 4/5 - Bare die**

----- Forwarded by Steve Pritchett/SaltLake/Fairchild on 04/21/99 06:32 PM -----

 Steve Pritchett  
04/21/99 03:40 PM

To: Rajeev Joshi/SantaClara/Fairchild@Fairchild, Ma Cristina B Estacio/Cebu/Fairchild@Fairchild, Consuelo N Tangpuz/Cebu/Fairchild@Fairchild, Honorio T Granada Jr/Cebu/Fairchild@Fairchild, Lester O Uy/Cebu/Fairchild@Fairchild  
cc: Steven Sapp/SantaClara/Fairchild@Fairchild, Bruce Marchant/SaltLake/Fairchild@Fairchild, John R Diroll/SaltLake/Fairchild@Fairchild, R Evan Bendall/SaltLake/Fairchild@Fairchild, Henry W Hurst/SaltLake/Fairchild@Fairchild, Annette Pieper/SaltLake/Fairchild@Fairchild, Gordon Madson/SaltLake/Fairchild@Fairchild  
Subject: Report 4/5 - Bare-die

I have broken this up into 4 emails/reports due to many photos.

1. Flipchip samples , some with gate to source shorts, some with black "corrosion" stain. (sent 4-19)
2. Wireless samples from Steve Sapp, SO-8 good/bad ?, identify cause of high Rdson. (sent 4-20)
3. SO-8 wireless samples prior to molding, sent per SL request to help understand leadframe layout.(sent 4-20)
4. **Bare die samples with bumps, sent per SL request.**
5. Samples of SOT-223 wireless parts sent to SV, construction analysis. (still in que)

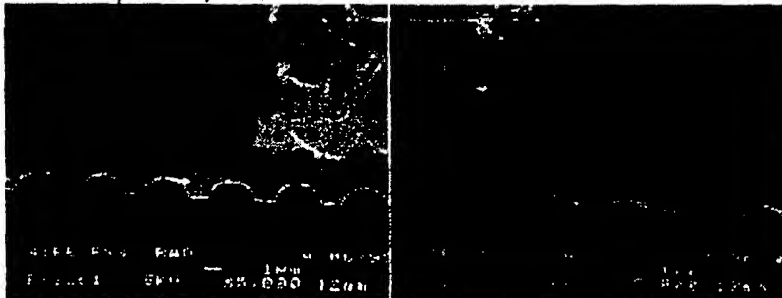
Wireless die samples, wafer Z009EM20KJ - 03 were sent from Cebu with objective of allowing SL to examine bumped die.

**SUMMARY - No UBM overlap. Some backside metal peel exhibited. D/A or pick operation causing backside chips.**

**Note: JPG files for these photos are available upon request.**

As received, the wafer had been bumped, backside metallization and diced. Also probe/sort/ink with most good-die already removed from film.

The following photos are observations. Cebu will need to access if these are problems, not representative of current process, etc.

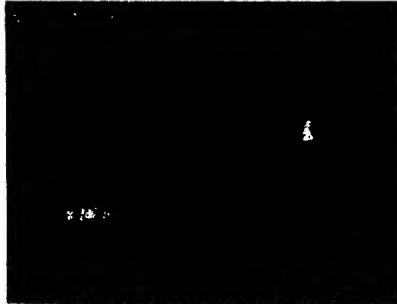


These 2 photos show opening, exposing Al metal, between passivation and UBM. Some Al erosion is present. UBM contact area nearly the same as passivation opening (no wedge of contamination or etch undercut). (die4.jpg & die3.jpg)





The chip of Si remaining on dicing film shows a repeated pattern. Since we have seen cracked die on 80-100V FA samples, concern was for chipped out die may be more susceptible to cracking. (die2.jpg)



A strip of backmetal peeled from portions of 3 die and remains on film. Concern is for FA samples where we have seen indications of missing or peeling backmetal. (die1.jpg)

The FA folks have suggested that assembly information/observations should be routine for builds going into reliability testing, especially if the die are being put in packages which require modified bonding or hand placement of die on lead frames. Example of this would be Dean's 100V parts which were put in non-standard package and had unique bonding. These (100V) parts had cracks and BMP. The assembly observations should be included with parts.

Thanks to Wayne Hurst and Annette Pieper for sample preparation, photos and input for this write-up. They are a little backed up for FA work at present.  
Thanks, Steve

***Cebu's comments:***


**Clemens Quinones 04/22/99 08:47 AM**

To: Steve Pritchett/SaltLake/Fairchild@Fairchild  
cc: Rajeev Joshi/SantaClara/Fairchild@Fairchild, Ma Cristina B Estacio/Cebu/Fairchild@Fairchild, Consuelo N Tangpuz/Cebu/Fairchild@Fairchild, Honorio T Granada Jr/Cebu/Fairchild@Fairchild, Lester O Uy/Cebu/Fairchild@Fairchild, Steven Sapp/SantaClara/Fairchild@Fairchild, Bruce Marchant/SaltLake/Fairchild@Fairchild, John R Diroll/SaltLake/Fairchild@Fairchild, R Evan Bendall/SaltLake/Fairchild@Fairchild, Henry W Hurst/SaltLake/Fairchild@Fairchild, Annette Pieper/SaltLake/Fairchild@Fairchild, Gordon Madson/SaltLake/Fairchild@Fairchild  
Subject: Report 2/5 - Wireless SO-8

Hi Steve,

Aside from the gross wafer bumping problems, cross-section photos below represents majority of the good SO-8 wireless units assembled using the old leadframe design (with U-groove/ mold compound

channel). U-grooving on topframe has more disadvantages than its desired purposes such as solder joint wicking when bumps happen to touch the edge of topframe contact pad, missing solder joint when solder reflow totally into u-grooves (mostly affects gate causing majority of test yield loss) and non-reflow of solder when the bump hides within the u-groove. Downset poor coplanarity of topframe's gate & source contact pads is also one of the causes why some bumps aren't reflowed well.

I decided to modify the leadframe design. U-grooves from topframe are removed and punch through holes are placed instead. Total volume of removed metal in the new design is almost equal to the volume removed due to U-grooving of old leadframe design. Pls click on icon for assessment details ->  Further assessment is done to check for solder wetting coverage, solder wicking, mold delamination and others.

Currently, all samples are still using the old leadframe design. Once the current WIP will be flushed out, the next batches of samples will be using the new leadframe design. Expected timeframe will be May.

Clemens

**Response**

**Subject:** >1st T am Meeting

**Response to:** TEAM MEETINGS

**Category:** Wireless SO-8 Pkg Dev't (Single Strand Approach)

**SOIC-8 WIRELESS 1ST TEAM MEETING**  
**<<<<< MINUTES OF THE MEETING >>>>>**  
**DATE : 23 FEB.'99**  
**TIME : 1530h**  
**VENUE : Synergy Room # 1**

|                                 |   |                                |
|---------------------------------|---|--------------------------------|
| <b><u>ATTENDEES:</u></b>        | Reynaldo Gandionco<br>(Prodn)           | Oliver Ledon (Assembly<br>COE) |
| Clemens Quinones<br>(PTG)       | Rusty Vega Jr. (F/E<br>Process Eng'g)   | Reynaldo Sondo (EOL<br>COE)    |
| Marvin Gestole (PTG)            | Emmanuel Livelo (F/E<br>Process Eng'g)  | Jun Soriba (EOL COE)           |
| Santos Mepieza (PTG<br>Support) | Noel Laylo (EOL & T/F<br>Process Eng'g) | Lester Uy (Rel & F/A)          |
| Rey Maligro (PTG<br>Support)    | Dexter Sorono (EOL<br>Process Eng'g)    | Rocil Tindugan (QA<br>Eng'g)   |
| Darwin Linao (PTG<br>Support)   | Allan Ermac (Fab<br>Process Eng'g)      | Engelbert Romero (QA<br>Eng'g) |

**AGENDA:**

1. WIRELESS PACKAGING HISTORY
2. SOIC-8 WIRELESS PKG. CONSTRUCTION
3. SOIC-8 WIRELESS FRONT END ASSY PROCESS FLOW
4. SOIC-8 WIRELESS EOL PROCESS FLOW
5. OPEN ISSUES

**DISCUSSIONS:**

- => wireless packaging brief history
- + wireless technology development started 1996 in SOT-223 pkg
  - + SO-8 wireless package development started June 1998.
  - + basic learnings in SOT-223 wireless package applied to SO-8 wireless pkg
  - + first SO-8 wireless prototyping attempt on matrix frame - very complicated and discontinued
  - + simultaneous development on single strand proven feasible and easy
  - + final approach to SO-8 wireless packaging is full sandwich assembly with overlapping top & bottom I/f
- => SOIC-8 wireless package construction
- DAP + D/A mat'l + Si trench die + solder bumps + gate & source terminal contacts + molded body
- => SOIC-8 wireless assembly process flow (Latest updates included)

**Front End Assembly Flow (Option #8)****1. SOFT SOLDER DIE ATTACH (ESEC 2005HR di attach)**

**Obstacle 1:** Die to topframe alignment not so good due to marginal DAP allowance for die placement. Missing gate balls (after reflow).

>> Modification of topframe required to allow bigger die placement tolerance and better die attach position/ placement. Remove U-grooves of topframe.

Resp. Clemens

Status: Changes incorporated in Rev. N topframe design.

FAI samples to arrive by March 31 yet.

**2.0 FLUX DISPENSING (ESEC cutter converted to flux dispenser)**

**Obstacle 2:** Flux distribution on die not good

>> flux dispensing tool need to conform die design. Fabricate flux dispensing tool designed for wireless dice (5A & 5F).

Resp. Clemens/ Bib/ Eman

Status: Awaiting final quotation from Micro-mechanics (vendor)

**3. TOP FRAME ATTACH**

**Obstacle 3:** Top Frame & bottom frame misalignment resulting to EOL problems.

>> Add bottom & top frame alignment press-fit studs & holes

Resp: Clemens

Status: Changes incorporated in Rev. P bottomframe &

Rev. N topframe design. FAI samples to arrive by March 31 yet

**Obstacle 4:** Topframe attach process currently on manual mode (along with rail spot welding process)

>> this process will be incorporated with the flux dispensing to avoid manual handling. ESEC cutter for flux dispensing will be annexed with auto top frame attach + rail stamping for press fitting stud & hole.

Resp: Santos & Oliver

Status: On going mechanical parts drafting & PLC program development

**4. RAIL SPOT WELDING (using tabletop leadframe alingment jig & C-clamp welding tips)**

**Obstacle 5:** Manual lithic process using a table top welding jig.

>> Longterm action item: Employ automated laser welding for non-contact welding

Resp: Marvin & Clemens

Status: Technical discusion with vendor is ongoing.

Purchase spec to be drafted. PPA to be generated yet.

**5. SOLDER REFLOW**

**Option 1: Using dixsealer (for small volume)**

**Obstacle 6:** No dedicated offline dixseal programmer

>> clone off-line programmer to be assembled before shipping out sold dixsealers to China. FSCB to use the clone programmer.

Resp: Bernard Benjamin & Edgar Baguio

Status: On going

**Option 2: Using conv yorized IR reflow oven (for mass production)**

**Obstacle 7:** IR oven process parameters not yet optimized.

>> process optimization to be done when more bumped wafers are available. More wafers available by WW42.

Resp: Clemens & R y M.

**End of Line Assembly Flow (Option #1)**

**6. MOLDING (2-chase mold mounted on Sumitomo press from SOT)**

**Obstacle 8:** In-house buy-off stage - molded strips encountered blown dambar & leads.

>> in-depth troubleshooting of molding process required.

Resp: Marvin/Dexter S/ Jun S

Status: SungWoo engineers to assist troubleshooting on day1-WW41.

**7. POST MOLD BAKE (1-hour)**

**Obstacle 9:** Prod'n favors no PMB. PMB is required to strengthen pkg surface to resist rough pkg during deflashing.

>> Eval required to determine the need for deflash jig.

Resp: Clemens & Darwin

Status: Eval on going

**8. DDD - Degate/Dejunk/Debar (share same press with TNF)**

**Obstacle 10:** Tool & Press still in Korea. Shipment is pending completion of TNF tool buy-off.

>> Expedite TNF tool buy-off.

Resp: Marvin

Status: Final leadformed units ongoing dimensional buy-off in Cebu. Press, DDD & TNF tool to be shipped to FSCB on WW41

**9. DEFLASH (Hitch with std SOT-23 plastic media deflasher. By May, one full-time plastic media deflasher will be released when other pkgs migrate to H2O jet deflash. )**

**Obstacle 11:** Are jigs required for deflashing? (See Obstacle 9) Which deflasher to convert?

>> Cyrus to identify what deflasher to convert. Deflash track & transport system to be fabricated.

Resp: Marvin & EOL COE

Status: Designing/ plans to start upon advise of Cyrus on what deflasher to use.

**10. LASER MARK**

**Option 1: Ride-on with YAG using strip carrier/ jig for small volume**

**Obstacle 12:** Jig design not suitable for jamming-free transport. Laser mark programming not yet done.

>> Jig modification required for steady vertical Y-axis leadframe support.

Resp: Clemens & Dexter S.

Status: Modified jig fabrication ongoing. Dexter to program laser marking with the modified jig.

**Option 2: Offline Strip Marker for mass production**

>> Retrieve strip marker from Covertek for transport mechanism modification

Resp: Rey S/ Jun S

Status: Retrieval of archived stripmarker - WW41

11. POSTPLATE (us SOT-23 plating racks & ride-on SO-8 platingline)

12. TRIM & FORM (share same press with TNF)

See DDD

=> other open issues:

1. Lay-out (Resp: Lyle)
2. Headcount allocation/forecast (Resp. Clemens)
3. Qual Plan/ Definition of requirements (Resp. Clemens)
4. Updated Cost/CLD (Resp. Clemens)
5. Documentations:
  - DFMEA (Resp: Clemens)
  - Prototype Control Plan (Resp: Clemens)
  - Pre-launch Control Plan (Resp: Clemens)
  - Qualification Plan (Resp: Clemens)
  - PCN required? (Resp. Clemens or SV)
  - Rejection Criteria (Resp. Arlene R.)
  - Process Specifications (Resp: Process Eng'rs)
    - Soft Solder D/A to Reflow = Eman
    - Molding to TNF = Dexter S.

June 4, 1999

Babak Sani, Esq.  
Townsend, Townsend & Crew  
Two Embarcadero Center, 8<sup>th</sup> Floor  
San Francisco, CA 94111

Re: Invention Disclosure entitled High Performance SOIC-8 DMOS  
Inventors: Maria Clemens Y. Quinones, et al.  
Our Reference No. 17732-9833


Dear Babak:

Enclosed is the above entitled invention disclosure for drafting into a patent application. There are several inventors involved in this application and they are all located in the Philippines. Rajeev Joshi will be the contact person here, so please contact Rajeev directly in Sunnyvale at 408.822.2163.

Please confirm receipt of this file and let me know the client matter number assigned. As with other files assigned to your firm, please include the FSC reference number on all documents/correspondence with copies to Pierce Atwood.

Thanks for your assistance.

Best regards,



Kate Oliver  
Administrative Associate, Legal

cc: Rajeev Joshi  
Chris Caseiro, Esq.

**TOWNSEND**  
*and*  
**TOWNSEND**  
*and*  
**CREW**

LLP

Denver, Colorado  
Tel 303 571-4000

Palo Alto, California  
Tel 650 326-2400

Seattle, Washington  
Tel 206 467-9600

**San Francisco**

Two Embarcadero Center  
Eighth Floor  
San Francisco  
California 94111-3634  
Tel 415 576-3200  
Fax 415 576-3300

Direct Dial 415 576-3300  
BSS@Townsend

June 7, 1999

Daniel E. Boxer, Esq.  
Executive Vice President, General Counsel  
and Chief Executive Officer  
FAIRCHILD SEMICONDUCTOR CORPORATION  
333 Western Ave., Mail Stop 01-00  
South Portland, ME 04106

Re: **VERTICAL MOSFET WITH ULTRA LOW-ON  
RESISTANCE AND GATE CHARGE PERFORMANCE**  
Your Ref: 17732-9827 / Our File: 018865-003300US  
**POWER MOS DEVICE WITH IMPROVED GATE  
CHARGE PERFORMANCE**  
Your Ref: 17732-9830 / Our File: 018865-003400US -- and --  
**HIGH PERFORMANCE SOIC-8 DMOS**  
Your Ref.: 17732-9833 / Our File: 018865-003500US

Dear Dan:

Receipt is confirmed of the referenced invention disclosures, for which we will begin with the preparation of patent applications. We will keep you apprised of the status of these matters. If you have any questions, please feel free to call.

Regards,



Babak S. Sani

BSS:deb

cc: Chris A. Caseiro, Esq.



9/20/99

- eliminate wire bond completely,
- placing another lead frame on top
- grooves are replaced by slots
- ~~the~~ spot welding to keep frames together
  - eg. 19 says cross fitting but actually now spot welding

**TOWNSEND**  
*and*  
**TOWNSEND**  
*and*  
**CREW**

LLP

Denver, Colorado  
Tel 303 571-4000

Palo Alto, California  
Tel 650 326-2400

Seattle, Washington  
Tel 206 467-9600

**San Francisco**  
Two Embarcadero Center  
Eighth Floor  
San Francisco  
California 94111-3834  
Tel 415 576-0200  
Fax 415 576-0300

November 19, 1999

***VIA FEDERAL EXPRESS***

Maria Clemens Y. Quinones  
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Re: Draft Patent Application  
For: IMPROVED METHOD OF MAKING A  
CHIP DEVICE  
Client Ref: 17732-9833  
Our File No.: 018865-003500US

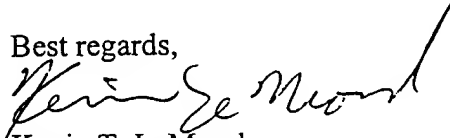
Dear Ms. Quinones:

Here is a draft of a patent application for the Improved Method Of Making A Chip Device, specifically, the patent application for the packaging of the high-performance SOIC-8 DMOS. You and the other inventors should review it carefully for content and accuracy. After you have done so, please provide me with any comments and changes that you may have. I will then incorporate them into the patent application so that we may file it with the U.S. Patent and Trademark Office.

Please note that in the disclosure, specifically, the drawing labeled "Part 4: Solder Bumps," reference is made to "UBM:TiW/Cu/Au or equivalent." I did not include this in the application since I am not clear as to what "UBM" refers. Thus, please provide me with this information so that I may include it in the patent application.

I look forward to hearing from you soon. Should you have any questions, please do not hesitate to contact me.

Best regards,

  
Kevin T. LeMond

KTL:rgH

Enclosure

cc: Daniel E. Boxer, Esq. (via U.S. Mail w/o encl.)  
Chris A. Caseiro, Esq. (via U.S. Mail w/o encl.)

**From:** "Clemens Quinones" <Clemens.Quinones@notes.fairchildsemi.com>  
**T :** "Kevin L Mond" <KTL@townsend.com>  
**Date:** Sun, Dec 5, 1999 5:09 PM  
**Subject:** Fairchild Ref. No. 17732-9833

Hi Kevin,

Greetings!

This is to inform you that I received the draft for patent application on IMPROVED METHOD OF MAKING A CHIP DEVICE. Thanks a lot for the enormous efforts done on drafting this document.

The item you left in majority of die & bump descriptions, i.e., the UBM, is an essential part of the solder bump structure. UBM stands for Under Bump Material. It is an intermediate layer between die & solder bump. Metallurgy for UBM cited for this patent is TiW/Cu/Au or equivalent. Attached drawing is example of UBM currently used for this package:

(See attached file: Die,UBM&bump\_structure.doc)

Die, UBM & solder bump always come as one in this patent application. For ease in description/nomenclature, we can call it collectively as "bumped die".

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During review of the draft, herebelow is the list of lines that are affected with above changes and other relevant corrections too.

(P refers to Page, L refers to Line)

P1,L31: change from "plurality of memory devices" to "plurality of DMOS devices"

P1,L32-P2,L1-4: (Pls change the description to match the bumped die description.)

P2,L17-19: (Pls change description to match the bumped die description. My suggestion- "In accordance with a further aspect of present invention, bumped dies are placed on topframe such that solder bumps are in direct contact with topframe.")

P3,L23: change from "perspective view of a top leadframe" to "perspective view of an inverted top leadframe"